AMENDMENTS TO THE CLAIMS

1. (currently amended) A method of forming an interconnect on a semiconductor substrate, comprising:

forming a relatively narrow first structure in a dielectric formed on a semiconductor substrate;

forming a relatively wider second structure in said dielectric ~~formed on the semiconductor substrate~~;

forming a liner in said relatively narrow first structure and said relatively wider second ~~structures~~ structure, such that a lower portion of said relatively narrow first structure is ~~substantially~~ completely filled ~~and said second structure is substantially unfilled~~ by said liner; and

forming a metallization over said liner to completely fill said relatively wider second structure.

2. (original) The method of claim 1, wherein said liner comprises one of a chemical vapor deposition (CVD) metal, a physical vapor deposition (PVD) metal and a plated liner.

3. (original) The method of claim 1, wherein said liner comprises at least one of tungsten, aluminum, and titanium nitride.

4. (original) The method of claim 1, wherein said metallization comprises copper.

5. (currently amended) A method of forming an interconnect on a semiconductor substrate, comprising:

forming a contact~~, including a slot,~~ in a dielectric formed on a semiconductor substrate;

forming troughs into the dielectric, thereby to form a dual damascene structure;

depositing a conducting material on the dielectric that completely fills a lower portion of the contact;

depositing a metal over the conducting material to completely fill the ~~slot and~~ troughs;

removing a portion of the metal ~~either to the conducting material or both the metal and the conducting material simultaneously back to the dielectric~~; and

selectively removing the conducting material.

6. (previously presented) The method of claim 5, wherein said dielectric comprises one of tetraethylorthosilicate (TEOS) oxide, silane oxide and another low K polymer dielectric.

7. (currently amended) The method of claim 6, wherein said ~~contacts comprise contacts~~ contact is formed between first and second metal levels formed on the semiconductor substrate.

8. (original) The method of claim 5, wherein said conducting material comprises tungsten.

9. (original) The method of claim 8, wherein the tungsten comprises chemical vapor-deposited (CVD) tungsten, a physical vapor deposition (PVD) tungsten, and a plated tungsten.

10. (currently amended) The method of claim 5, wherein a thickness of the conducting material is adjusted so as to ~~substantially~~ completely fill the ~~relatively small contacts~~ the lower portion of the contact.

11. (original) The method of claim 5, wherein said metal comprises copper.

12. (original) The method of claim 5, wherein the metal is removed by chemical mechanical polishing (CMP).

13. (original) The method of claim 5, wherein said selectively removing comprises selectively removing said conductive material by a selective etch.

14. (original) The method of claim 5, wherein said selectively removing comprises selectively removing said conductive material by a selective CMP.

15. (previously presented) The method of claim 5, further comprising:

repeating said depositing a conducting metal; and

repeating said depositing a metal over the conducting material, thereby depositing subsequent said conducting material and said metal on the resulting structure.

16. (currently amended) A method of forming an interconnect on a semiconductor substrate, comprising:

forming troughs between first and second metal levels, including a slot, in a dielectric formed on a semiconductor substrate;

forming contacts in the dielectric, thereby to form a dual damascene structure;

depositing a conducting material on the dielectric, said conducting material completely filling a lower portion of said dual damascene structure;

depositing a metal over the conducting material to completely fill the slot and the troughs;

removing a portion of the metal ~~either to the conducting material or both the metal and the conducting material simultaneously back to the dielectric~~; and

selectively removing the conducting material.

17. (withdrawn) A semiconductor device, comprising:

a semiconductor substrate;

a dual damascene structure formed in at least one dielectric film formed on the semiconductor substrate, including a relatively narrow first structure and a relatively wider second structure;

a liner formed in said first and second structures such that said first structure is substantially filled and said second structure is substantially unfilled; and

a metallization formed over said liner to completely fill said second structure.

18. (previously presented) The method of claim 16, wherein said conducting material comprises one of a chemical vapor deposition metal, a physical vapor deposition metal, and a plated liner.

19. (currently amended) The method of claim 16, wherein said ~~contacts comprise contacts~~ contact is formed between first and second metal levels formed on the semiconductor substrate.

20 (previously presented) The method of claim 16, wherein said selectively removing comprises selectively removing said conductive material by a selective etch.

21. (previously presented) The method of claim 1, wherein said relatively narrow first structure is not connected on said substrate to said relatively wider second structure.

22. (previously presented) The method of claim 1, wherein said forming a relatively wider second structure forms said wider structure on said substrate apart from said relatively narrow structure.

23. (previously presented) The method of claim 5, wherein said contact is not connected in said substrate to said trough.

24. (previously presented) The method of claim 16, wherein said forming troughs forms said troughs in said dielectric apart from said contact.

25. (new) The method of claim 16, wherein said contact comprise a depth of a range from

about 2000 Å to about 8000 Å.